Module Introduction

PURPOSE:
The intent of this module is to provide an overview of the HCS12.

OBJECTIVES:
- Describe the main features of the HCS12.
- Identify HCS12-family derivatives.
- Identify derivative availability.
- Describe the basic architecture and programming model of the HCS12.
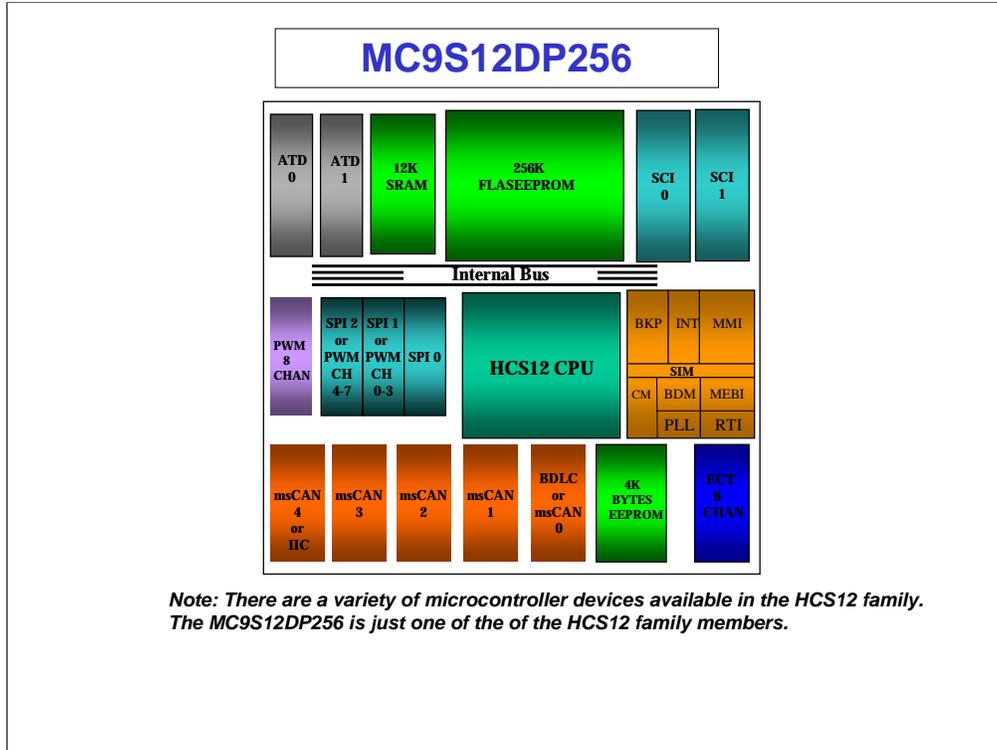
CONTENT:
- 26 pages
- 4 questions

LEARNING TIME:
- 50 minutes

The intent of this module is to provide an overview of the HCS12. You will become familiar with the main features of the HCS12, as well as HCS12-family derivatives. You will also learn about derivative availability. Finally, you will explore the basic architecture and programming model of the HCS12.

MC9S12DP256

| ATD 0 | ATD 1 | 12K SRAM | 256K FLASEEPROM | | SCI 0 | SCI 1 |

Internal Bus

PWM 8 CHAN	SPI 2 or PWM CH 4-7	SPI 1 or PWM CH 0-3	SPI 0	HCS12 CPU	BKP	INT	MMI
					CM	SIM BDM	MEBI
						PLL	RTI

| msCAN 4 or IIC | msCAN 3 | msCAN 2 | msCAN 1 | BDLC or msCAN 0 | 4K BYTES EEPROM | ECT 8 CHAN |

Note: There are a variety of microcontroller devices available in the HCS12 family. The MC9S12DP256 is just one of the of the HCS12 family members.

Let's begin with an overview of the MC9S12DP256 microcontroller unit (MCU). The MC9S12DP256 is one of the many derivatives that are currently available in the HCS12 family. This device contains a large amount of on-chip memory and peripheral I/O devices.

The MC9S12DP256 is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 256K bytes of Flash EEPROM, 12K bytes of RAM, and 4K bytes of EEPROM.

The MC9S12DP256 is also composed of 2 asynchronous Serial Communications Interfaces (SCI), three Serial Peripheral Interfaces (SPI), and an enhanced capture timer with 8 Input Capture/Output Compare (IC/OC) channels.

You can see that this device contains two 8-channel, 10-bit Analog-to-Digital Converters (ADC), and an 8-channel Pulse-width Modulator (PWM).

The MC9S12DP256 is also composed of a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), and 20 discrete digital I/O lines with interrupt and wakeup capability. This MCU has five CAN 2.0 A, B software compatible modules (MSCAN12) and an Inter-IC Bus.

Here you can see the System Integration Module (SIM). It manages the system resource mapping, clock generation, interrupt control and bus interfacing, etc.

The MC9S12DP256 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a Phase Locked Loop (PLL) circuit allows power consumption and performance to be adjusted to suit operational requirements.

Main Features

16-bit HCS12 CPU
- Upward compatible with HC11/12 instruction set
- Interrupt stacking and programmer's model identical to HC11/12
- 20-bit ALU
- Instruction pipe
- Enhanced indexed addressing

System Integration Module (SIM)
- Multiplexed External Bus Interface (MEBI)
- Module Mapping Control (MMC)
- Interrupt Control (INT)
- Breakpoints (BKP)
- Background Debug Mode (BDM)

Clocks and Reset Generator (CRG)
- -- Low current oscillator, PLL, reset, clocks, COP watchdog, real-time interrupt, clock monitoring

Memory
- Split Gate Flash EEPROM (paged)
- Split Gate EEPROM (word write, two-word erase)
- Zero wait state RAM

Mouse over the headings to learn more about the main features of the HCS12 family.

Peripherals
- Enhanced Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- 1M bit per second, CAN 2.0 A, B msCAN module (with paged message buffers)
- Universal Serial Bus 2.0 (USB) interface
- Byte Data Link Controller (BDLC)
- Inter-IC Bus (IIC)
- 10-bit Analog-to-Digital Converter (ADC)
- Standard 8-channel timer
- Enhanced Capture Timer (ECT)
- PWM module
- Stepper motor controller
- LCD controller

On-chip Voltage Regulator
- 2.25V to 2.75V digital supply voltage generated using an internal voltage regulator
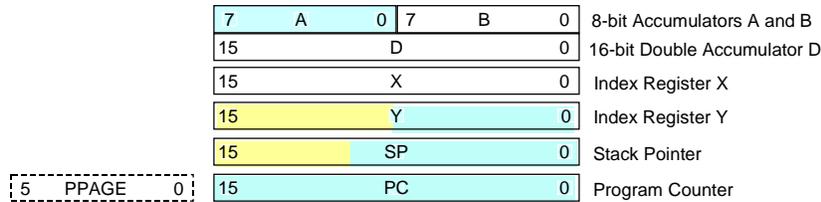- 4.75V to 5.25V analog and I/O supply voltage

Technology: 0.25 micron CMOS
- 50 MHz CPU equivalent to 25 MHz bus operation (66/33 MHz in design)

Roll your mouse pointer over each of the headings to learn more about the main features of the HCS12 family.

HCS12 Programmer's Model

68HC11 = 68HC12 = HCS12 Programmer's Model

| 7 | A | 0 | 7 | B | 0 | 8-bit Accumulators A and B |

15	D	0	16-bit Double Accumulator D
15	X	0	Index Register X
15	Y	0	Index Register Y
15	SP	0	Stack Pointer
15	PC	0	Program Counter

5 PPAGE 0

7 0
S X H I N Z V C   Condition Code Register

- Carry/Borrow (from MSB)
- Overflow
- Zero
- Negative (MSB = 1)
- I - Interrupt Mask
- Half Carry (for BCD)
- X - Interrupt Mask
- STOP Disable

- ◆ **Source code compatible**
- ◆ **Identical stack frame**
- ◆ **PPAGE used by CALL and Return To Call (RTC) (paged HC(S)12 only)**
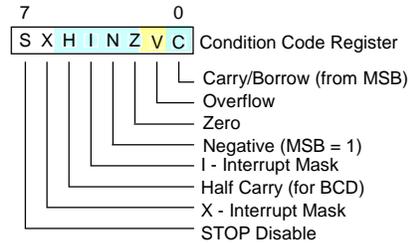
HC05 / HC08 / HCS12
HC08 / HCS12

Here, we can see the HCS12 programmer's model. This programming model is identical to the HC11 and HC12. With this model, the PPage register is used to allow access to more than 64K of memory space by the CPU. The Flash is accessed in 16 pages by controlling the PPAGE register via the call and return from call (RTC) instructions. A Flash page can be accessed manually by writing the PPAGE register with the page number.

Question

Is the following statement true or false? Click "Done" when you are finished.

"System resource mapping, clock generation, interrupt control and bus interfacing are managed by the System Integration Module (SIM)."

True

False

Consider this question regarding the main features of the HCS12 family.

System resource mapping, clock generation, interrupt control and bus interfacing are managed by the System Integration Module (SIM). The HCS12 family has full 16-bit data paths throughout.

HCS12 Serial Interface Features

• **Modular architecture allows future expansion**

• **Pins may be configured as general purpose I/O**

• **Loop mode operation for debugging**
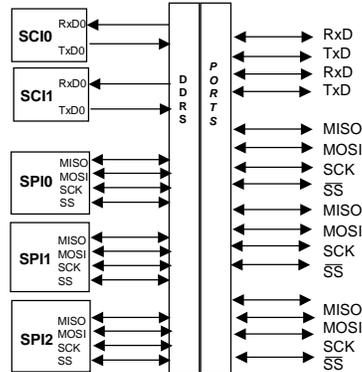
Now, let's take some time to look at some of the HCS12 features in more detail.
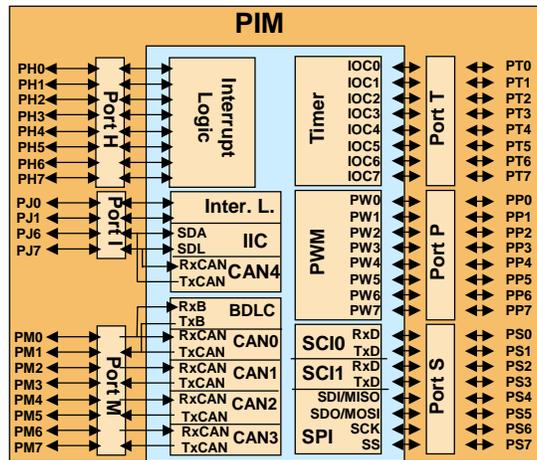
SCI and SPI are both HCS12 serial interfaces. The SCI is an asynchronous communication port with a 13-bit break support. The SCI is ideal for off-board serial communication and may be used to interface to a modem or drive an RS232 device.

The SPI is a synchronous high-speed communication port. It is a high-speed interface that may be used to communicate with other MCUs, an ADC, a DAC, an LCD, a seven segment display, and many more.

The SCI and SPI have a single-wire function. With enhancements, these two serial interfaces are similar to the MC68HC11. Here, we can see some of the features of both the SCI and SPI.

MC9S12 Enhanced Capture Timer

Here, we can see an example of the MC9S12 ECT, which is another feature of the HCS12. The MC9S12 ECT contains a 16-bit timer with a 7-bit prescaler. It has eight Input Capture (IC)/Output Compare (OC) channels, four of which are buffered Input Capture channels. It also includes a 16-bit modulus down-counter with a 4-bit prescaler. The 16-bit modulus counter may be used to facilitate a periodic interrupt time base and control the Input Capture (IC)/Pulse Accumulator (PA) register latching mechanism.

The MC9S12 ECT also includes four 8-bit or two 16-bit pulse accumulators. Independent interrupt sources for the MC9S12 ECT include eight IC/Ocs, a Timer Overflow, three Pulse Accumulator and a Modulus Counter. Finally, this HCS12 feature contains four inputs with selectable delay counters that are used to filter out spurious signals.

Port Integration Module

The Port Integration Module (PIM) is a standardized interface between peripheral modules and I/O pads for all ports, with the exception of ports A, B, E, and K. These ports are part of the core. The port control functions within the standard peripheral modules are removed.

The PIM controls the attributes of a port, such as pull-up and reduced drive, regardless of whether it is used for general purpose I/O or a special function. The exception to this is that some modules, such as SPI, may override pin direction and data settings in the PIM.

Click "Port Features" to learn about some standard port features.

Standard Port Features

Standard port features:

- User-defined "electrical" characteristics on a pin-by-pin basis:
  – Reduced drive
  – Wired-OR mode
  – Pull-ups/downs*

  (*Certain precautions are taken with pull-ups/downs. If the msCAN bus is enabled, a pull-up is allowed, but a pull-down is blocked.)

- High flexibility (Port registers are relocatable in the memory map.)

[This is a reference page for the "Port Features"]

IIC Features

- Is I^{2}C bus standard compatible
- Has a multi-master operation
- Is software programmable for one of 256 different serial clock frequencies
- Contains a software selectable acknowledge bit
- Contains interrupt driven byte-by-byte data transfer
- Has an arbitration lost interrupt with automatic mode switching from master to slave
- Contains a calling address identification interrupt
- Provides for start and stop signal generation/detection
- Provides for repeated start signal generation
- Provides for acknowledge bit generation/detection
- Has bus busy detection
- Supports low power modes
- Is shared with the msCAN 4

Another feature of the HCS12 is the Inter-IC (IIC) interface. This interface is used extensively in radio applications. Here, we can see a vast number of IIC features.

Question

The HCS12 has a number of distinct features. Match each feature with its description by dragging the letters on the left to their corresponding items on the right. Click "Done" when you are finished.

| A | SCI | C | A component that contains a 16-bit timer with a 7-bit prescaler and eight IC/OC channels |
B	SPI	E	An interface used extensively in radio applications
C	MC9S12 ECT	A	An asynchronous communication port with a 13-bit break support
D	PIM	D	A standardized interface between peripheral modules and I/O pads for most ports
E	IIC	B	A synchronous high-speed communication port

| Done | Reset | Show Solution |

Let's review some of the HCS12 features.

The SCI is an asynchronous communication port with a 13-bit break support. The SPI is a synchronous high-speed communication port. The MC9S12 ECT contains a 16-bit timer with a 7-bit prescaler. It has eight IC/OC channels, and four of the IC channels are buffered. The PIM is a standardized interface between peripheral modules and I/O pads for all ports, with the exception of ports A, B, E, and K. Finally, the IIC is used extensively in radio applications.

msCAN Bus

CAN Numbering Order	
1 CAN	CAN0
2 CANs	CAN0, CAN4
3 CANs	CAN0, CAN4, CAN1
4 CANs	CAN0, CAN4, CAN1, CAN2
5 CANs	CAN0, CAN4, CAN1, CAN2, CAN3
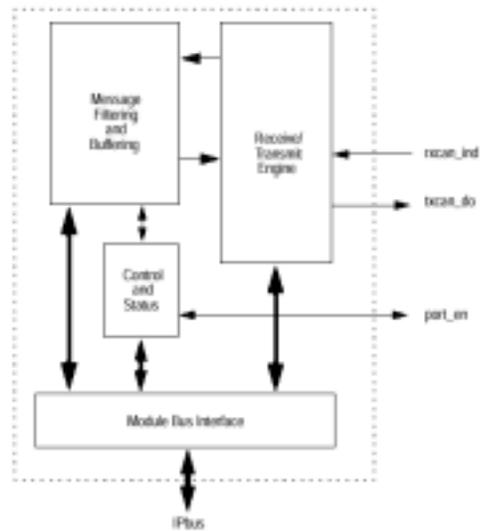
The msCAN is a Serial Communication Interface developed by Bosch corporation. The msCAN bus is targeted for automotive and industrial applications that support part A and part B.

Five CAN modules are available on the HCS12, which provide the system with multiple receive and transmit buffers. In the table, you can see the CAN numbering order for parts with various numbers of CAN modules.

It is important to note here that the msCAN0 is multiplexed with the Byte Data Link Controller (BDLC), and the msCAN4 is multiplexed with the IIC.

Click "Features" to view some of the central features of the msCAN bus.

msCAN Bus Features

- **Can have up to 5 msCAN modules**

- **Contains 3 Tx message buffers, each automatically mapped**

- **Contains 5 background Rx buffers**

- **Has programmable I/O modes**

- **Has maskable interrupts**

- **Has programmable loopback for self-test operation**

- **Is independent of the transmission medium (external transceiver is assumed)**

- **Contains an open network architecture**

- **Is a multi-master concept**

- **Has a high immunity to EMI**

- **Has a short latency time for high-priority messages**

- **Contains low power sleep mode, with programmable wakeup on bus activity**

[This is a reference page for the "Features"]

BDLC (J1850)

- **Is SAE J1850 compatible**

- **Contains a 10.4 Kbps Variable Pulse Width Modulation (VPW) bit format**
- **Contains a digital noise filter**
- **Provides for collision detection**
- **Allows for hardware CRC generation/checking**
- **Supports receive and transmit block mode**
- **Supports 4X receive mode (41.6 Kbps)**
- **Contains a digital loopback mode**
- **Supports In-Frame Response types 0, 1, 2, and 3**
- **Provides for power-saving stop and wait modes with automatic wakeup on network activity**
- **Supports interrupt generation with vector look-up table**

The BDLC or J1850 is another feature of the HCS12. Like the msCAN bus, this feature is also targeted for automotive applications. However, the BDLC operates at a much lower bus speed than the CAN interface.

Parts with "J" in the part number generally have a J1850 interface, 9S12DJ64 for example. Here, we can see a number of BDLC (J1850) features.

Analog-to-Digital Converter
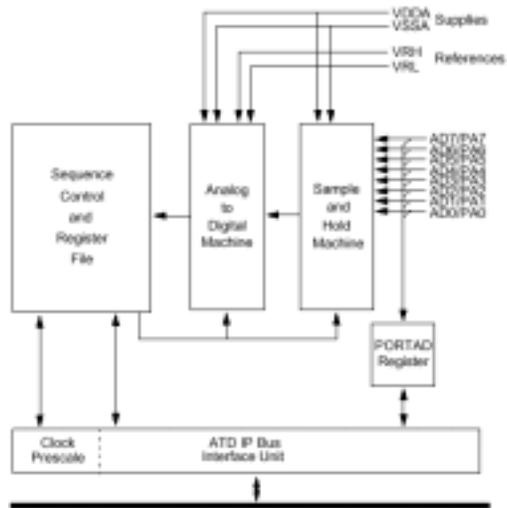
Click "ADC Features" to view some of the features of an Analog-to-Digital Converter (ADC).

ADC Features

- Has an 8/10-bit resolution

- Has a 7 usec, 10-bit single conversion time

- Contains a sample buffer amplifier

- Provides for programmable sample time

- Is left/right justified and contains signed/unsigned result data

- Has an external trigger control

- Provides for conversion completion interrupt generation

- Has an analog input multiplexer for 8 analog input channels

- Provides for Analog/Digital input pin multiplexing

- Has 1 to 8 conversion sequence lengths

- Provides for continuous conversion mode

- Contains multiple channel scans

[This is a reference page for the "ADC Features"]

PWM Features
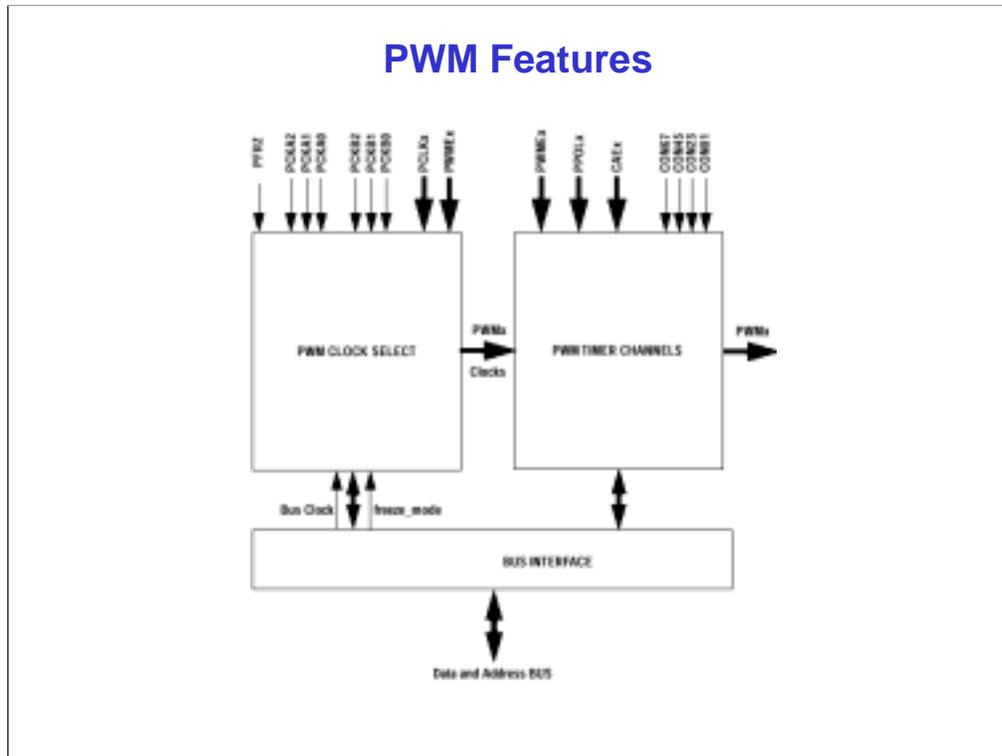
The Pulse Width Modulator (PWM) has a number of important features. Most notably, it has eight independent PWM channels with programmable period and duty cycles. These period and duty cycles are double buffered. The PWM is configurable as 8-bit eight channels or 16-bit four channels.

The PWM contains a flexible clock generation (A, B, SA, and SB) that covers a wide range of frequencies. It also allows for immediate PWM updates, and the polarity is software selectable. The PWM contains a programmable center or left-aligned PWM output.

The PP7 pin in the PWM can be used to shut down all of the PWM channels in the event that the hardware senses an over-current or over-temperature condition.

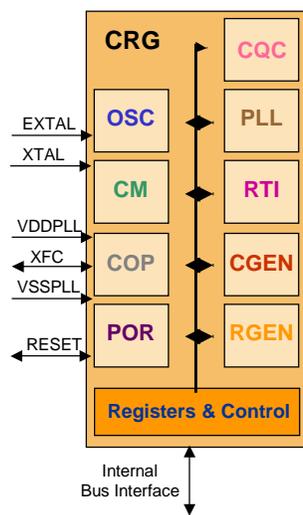Complete this question which tests your knowledge of different HCS12 features.

The msCAN bus is a serial communication interface developed by the Bosch Corporation. The msCAN bus is targeted for automotive and industrial applications that support part A and part B.

HCS12 Device Identification

Coding	
Bit 15-12	Major family identifier
Bit 11-8	Minor family identifier
Bit 7-4	Major mask set revision number, including FAB transfers
Bit 3-0	Minor (non-full) mask set revision

Some tools, such as the BDMPGMR12 and DBug12, read the device ID in order to automatically configure themselves for the correct device. The part ID is located in two 8-bit registers, PARTIDH and PARTIDL. The read-only value is a unique part ID for each revision of the die. The device memory size is also located in two 8-bit registers, MEMSIZ0 and MEMSIZ1.

MC9S12 Clock and Reset Generator

Mouse over the light orange boxes to learn more about CRG components.

CRG

CQC

OSC | PLL

CM | RTI

COP | CGEN

POR | RGEN

Registers & Control

EXTAL
XTAL
VDDPLL
XFC
VSSPLL
RESET

Internal Bus Interface

- **Crystal Oscillator (OSC): Colpitts with translated GND (as per HC12D-family) or traditional Pierce configurations**
- **Clock Monitor (CM): Same as on the HC12D-family**
- **Clock Quality Checker (CQC): Ensures valid clock for operation**
- **Phase Locked Loop (PLL): The same as on the HC12D-family**
- **System Clocks Generator (CGEN) simplified clock chain:**
  - **Core Clock = PLLCLK or OSCCLK**
  - **Peripherals Clock = PLLCLK/2 or OSCCLK/2 (25% duty)**
  - **ECLK = PLLCLK/2 or OSCCLK/2 (50% duty)**
  - **No Slow Mode Clock**
- **System Reset Generator (RGEN): Same reset functionality as on the HC12D-family. Reset by Power-On Reset POR, COP, Ext. Reset, Clock and Clock Monitor**
- **Real-Time Interrupt (RTI): Slightly different divider chain**
- **Watchdog (COP): Slightly different divider chain**
- **Power-On Reset (POR): Allows the oscillator to stabilize**

The MC9S12 Clock and Reset Generator (CRG) is a low power oscillator that supports operations of up to 33 MHz. Most HCS12 parts allow Colpitts and Pierce oscillator configurations. The Colpitts configuration is good for lower power and lower EMI, but it is limited to 0.5 to 16 MHz crystal/resonators. The Pierce configuration uses more power and has higher emissions, but allows up to 40 MHz crystal/resonators. Generally, the Colpitts is a better choice because the PLL can be used to increase the bus frequency to the maximum allowed (25 MHz currently).

Self clock mode may be used by the application to allow the MCU to continue to run at a much less accurate frequency in case the reference clock become malfunctioned. You will learn more about this later. Roll your mouse pointer over the light orange boxes to learn more about CRG components.

MC9S12 Low Power Modes

- RUN Mode (full operation)

- WAIT Mode (CPU is sleeping)

- STOP Mode (all modules stopped)

- Pseudo STOP Mode (all modules stopped)

The MC9S12 CRG is a low power oscillator design that is engineered to avoid power-wasting harmonics. It also contains user-configurable, low-power peripheral modes.

RUN mode is full operation at a maximum of 65 mA. With this mode, peripherals will automatically shut down if they are not in use.

WAIT mode is entered when the CPU executes the Wait Instruction, WAI. With this mode, peripherals can be configured to shut down as the CPU enters this mode. It operates at a maximum of 40 mA when all of the modules are enabled, and a maximum of 5 mA when only the Real-Time interrupt is enabled.

STOP mode means that all of the modules (oscillator, PLL and all peripherals, etc.) are stopped. It typically operates at 30 uA (at 27°C).

Pseudo STOP mode also means that all of the modules are stopped. It typically operates at 350 uA (at 27°C). However, the oscillator runs in low power mode, which enables a fast wakeup, comparable to that in Stop mode. For most designs, where low power is required, Pseudo STOP (PSTOP) mode is a good choice because the fast wakeup allows the oscillator to stay running.

HCS12 Resets

Power-On Reset (POR)

- Special delayed reset

- Releases above 2.07V

- Active below 0.97V

- Clock quality check window of 50 self-clock cycles

- Cause of last reset can be checked

A Power-On Reset (POR) is a special delayed reset that allows the oscillator to stabilize. However, POR does not replace Low Voltage Inhibit (LVI) functions. The HCS12 does not include the LVI circuit. The LVI or equivalent circuit needs to be supplied externally, and is application dependant. Usually, an external Low Voltage Reset circuit is needed to reset a part when the Vdd drops below the point at which the core is guaranteed to operate.

POR releases when the Vdd2.5 goes above 2.07V and is active when the Vdd2.5 goes below 0.97V.

With POR, the clock quality check window is 50K self clock cycles. If the oscillator amplitude and frequency are sufficient for 4,096 cycles to be detected during a quality check window, then the POR is exited using the XTAL clock. Up to 50 quality check windows can occur if the oscillator is slow to start. However, after 50 unsuccessful tries, Self Clock Mode is entered.

The POR bit can be checked for the cause of the last reset, and it can only be cleared via software.

MC9S12 System Integrity

Roll your mouse pointer over each element to learn more about MC9S12 system integrity.

- **Clock Monitor Function**
- Detects crystal failure and takes user-specified action > bad clock detect

- **Clock Quality Checker**
- Performs a window check on the oscillator to ensure that the MCU only executes from a stable clock > good clock detect

- **Self Clock Mode (SCM)**
- Provides for limited operation even with temporary crystal problem
- Allows controlled shutdown in the event of oscillator failure
- Allows for slow startup of crystal oscillators
- Allows for robust system design where the MCU can continue to operate and do controlled shutdown, or diagnostics, even if the crystal fails
- Has a frequency of 1 to 5.5 MHz

- **Flexible Watchdog (COP)**
- Can be used as "windowed" COP (only refresh between 75%-100% of the period)
- Further reduces the possibility of code runaway
- Is independent from the PLL (clocked directly from crystal) and secure even if the PLL fails

The integrity of the MC9S12 system relies on a number of elements, four of which are presented here. Roll your mouse pointer over each element to learn more about MC9S12 system integrity.

Background Debug Mode

BDM on the MC9S12:

- Provides for low cost serial real-time emulation and debug

- Can single step, run, or stop the application code

- Contains on-chip hardware for multiple breakpoints

- Replaces expensive emulators or bus analyzers

- Works at full operating voltage and frequency range

- Is non-intrusive (there is no cumbersome emulator cables)

- Has in-circuit Flash/EE programming

As part of the MC9S12, Background Debug Mode (BDM) can be used for end-of line programming of Flash and EEPROM. It can also be used to complete debug in the end application. For complex debugging that requires TRACE (logic analyzer) functionality or lots of hardware breakpoints, an In-Circuit Emulator (ICE) is required. Take a moment to look over some of the BDM features that are presented here.

MC9S12 0.25u Flash

Highly Flexible:

- 5 volt Flash (no external charge pump is required)
- Market-leading Flash granularity (512B Flash Erase / 2B Program)
- Virtual EEPROM implementation possible for EE extension
- Four independently programmable Flash Segments (DP256) that can erase one block while reading another

High Speed Programming:

- Fast Flash Page Erase (20 ms or 512 bytes)
- Can program 16 bits in 50 us
- Total Program Time for 128K code down to less than 5 seconds

Efficient end-of-line programming possible

The MC9S12 0.25u Flash is the best in the industry. Most notably, it contains a built-in state machine for Flash programming that controls sequence and timing. It should also be noted that once a user sets the FDIV register to get the correct clock frequency to the Flash module, PROGRAM and ERASE are simple commands to the state machine. Spend some time looking over the characteristics of the MC9S12 0.25u Flash that are presented here.

If you would like to find out more about the MC9S12 0.25u Flash, we recommend reading AN2204: "Fast NVM Programming for the HCS12P256."

HCS12 Power Supplies

- **Vddr**   Supplies regulator and ports A, B, E, and H - connect to 5V and bypass with 100 nF

- **Vdd1, 2**   Outputs from 2.5V regulator; supply core - bypass with 47-220 nF depending on EMC results.

- **Vddpll**   Output from 2.5V regulator; supplies Osc. and PLL - bypass with 22-100 nF

- **Vdda**   Supply to A/D; connect to 5V and bypass with 22-100 nF

- **Vrh**   Reference for A/D; connect to 5V and bypass with 10 nF

- **Vddx**   Supply for all ports except those supplied by Vddr; connect to 5V and bypass with 47-220 nF. Add 10 uF if big loads are switched.

Here is a look at the HCS12 power supplies. Vdd1, Vdd2, and Vddpll are 2.5V outputs from the internal regulator and should only be bypassed to ground. Do not connect 5V to these pins! To see a table of Absolute Maximum Ratings for the HCS12 power supplies, click "Ratings".

Ratings

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.0	V
7	Analog Reference	V_{RH}, V_{RL}	-0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [3]	I_D	-25	+25	mA

Note: **The HCS12 has a steady-state injection current rating of 2.5 mA per pin and 25 mA per package.**

[This is a reference page for the "Ratings"]

Question

Which of the following are MC9S12 low power modes? Select all options that apply.

RUN mode

Pseudo STOP mode

STOP mode

RESUME mode

WAIT mode

Let's take a moment to review the MC9S12 low power modes.

The MC9S12 has four low power modes: RUN mode (full operation), WAIT mode (CPU is sleeping), STOP mode (all modules stopped including oscillator), and Pseudo STOP mode (all modules stopped except Oscillator).

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Module Summary

- HCS12 Main Features
- HCS12-family Derivatives
- Derivative Availability
- HCS12 Basic Architecture
- HCS12 Programming Model

Now that you have completed this module, you should be able to describe a variety of HCS12 features, from the HCS12 serial interfaces to the different HSC12 power supplies. You should also be able to describe the HCS12-family derivatives, as well as derivative availability. Finally, you should be able to outline the basic architecture and programming model of the HCS12.